CLAIMS

We claim:

1. An improved capacitive sensing circuit comprising:

a sense pulse generator providing a first polarity sense pulse and a second polarity sense pulse;

a sense capacitor coupled to the sense pulse generator;

a detector coupled to the sense capacitor; and

a storage device coupled to the detector.

2. The circuit of claim 1 wherein the storage device is a sample and hold circuit.

3. The circuit of claim 2 wherein the sample and hold circuit further comprises an amplifier and a capacitor.

4. The circuit of claim 1 wherein the storage device comprises a capacitor.

5. The circuit of claim 1 further including a filter coupled to the storage device.

6. The circuit of claim 1 wherein the sense pulse generator provides said first polarity sense pulse over a first phase and said second polarity sense pulse over a second phase.

7. The circuit of claim 6 further including a demodulation circuit coupled to the storage device.

8. The circuit of claim 7 wherein said demodulation circuit comprises a filter having an input and an output, and a nonlinear element having a first input, wherein said nonlinear element is selected from one of the following: a switch, a multiplier, a mixer.

9. The circuit of claim 8 wherein said filter includes a high-pass characteristic and said filter output is coupled to said first input of the nonlinear element.

10. The circuit of claim 8 wherein said filter includes a low-pass characteristic, said nonlinear element includes an output, and said filter input is coupled to said output of the nonlinear element.

11. The circuit of claim 8 wherein said nonlinear element further includes a second input coupled to a signal synchronous with sense pulse polarity.

12. The circuit of claim 8 wherein said demodulation circuit further comprises an input and an output, and an analog signal is provided to said demodulation circuit input.

13. The circuit of claim 8 wherein said demodulation circuit further comprises an input and an output, and a digital signal is provided to said demodulation circuit input.

14. The circuit of claim 1 further including a second sense capacitor coupled to the detector and the sense pulse generator.

15. The circuit of claim 14 further including a third and a fourth capacitor coupled to the detector and the sense pulse generator,

wherein said sense pulse generator generates a first set of sense pulses on the first through fourth sense capacitors and a second set of sense pulses on the first through fourth sense capacitors.

16. The circuit of claim 15 wherein the first, second, third and fourth capacitors form a portion of a microstructure, and said detector comprises an output, said output being responsive to the orientation of said microstucture.

17. The circuit of claim 1 further including an analog to digital converter coupled to the storage device.

18. The circuit of claim 17 further including a demodulator coupled to the output of the analog to digital converter.

19. The circuit of claim 1 wherein said first sense pulse comprises a voltage pulse, and said second sense pulse comprises a voltage pulse.

20. The circuit of claim 1 wherein said first sense pulse comprises a charge pulse, and said second sense pulse comprises a charge pulse.

21. The circuit of claim 1 wherein said detector comprises a charge detector.

22. The circuit of claim 1 wherein said detector comprises a voltage detector.

23. A sampled data system having two phases, comprising:

at least a first sense transducer, said sense transducer comprising an output;

a first phase sampling said output of the sense transducer;

a second phase sampling said output of sense transducer, the difference between first and second samples providing a measurement of the position of a body coupled to the sense transducer; and

a sense pulse generator providing a sense pulse to the sense transducer, the generator providing a first polarity of said sense pulse to said sense transducer during a first incidence of said first phase and said second phase, and a second polarity of said sense pulse to said sense transducer during a second incidence of said first phase and said second phase.

24. The system of claim 23 further including a second sense transducer coupled to the sense pulse generator and receiving a sense pulse having the first polarity during a third incidence of said first and said second phase, and a sense pulse having the second polarity during a fourth incidence of said first and said second phase.

25. The system of claim 24 wherein the first sense transducer and the second sense transducer are coupled to a body having at least a first and a second degree of movement, the first sense transducer coupled to detect a change in said first degree of movement and the second sense transducer coupled to detect a change in said second degree of movement.

26. The system of claim 24 wherein the polarity of said sense pulse is controlled by a digital modulation signal.

27. The system of claim 23 further including a charge integrator coupled to the output of the sense transducer.

28. The system of claim 27 further including a storage device coupled to the output of the charge integrator.

29. The system of claim 28 further including a demodulator coupled to the output of the storage device

30. The system of claim 23 further including a buffer coupled to the output of the sense transducer.

31. The system of claim 30 further including a storage device coupled to the output of the buffer.

32. The system of claim 31 further including a demodulator coupled to the output of the storage device.

33. The system of claim 23 further including a charge detector coupled to the output of the sense transducer.

34. The system of claim 33 further including a storage device coupled to the output of the charge detector.

35. The system of claim 34 further including a demodulator coupled to the output of the storage device.

36. A circuit, comprising:

a sense capacitor coupled to a microstructure;

a charge detector coupled to the sense capacitor;

a sense pulse generator coupled to said sense capacitor, said sense pulse generator comprising control circuitry, said control circuitry causing the sense pulse polarity to invert over two phases; and

sense circuitry coupled to the charge detector detecting the difference between the phases.

37. The circuit of claim 36 wherein the charge detector comprises a buffer amplifier.

38. The circuit of claim 36 wherein the charge detector comprises a charge integrator.

39. The circuit of claim 36 wherein the sense circuitry comprises:

a storage device coupled to the charge detector;

a demodulator coupled to the storage device.

40. The circuit of claim 36 further including:

a storage device coupled to the charge detector;

an analog-to-digital converter coupled to the output of the storage device; and

a digital demodulator coupled to the analog-to-digital converter.

41. An optical mirror switch, comprising:

an optical mirror assembly;

at least one sense capacitor coupled to the optical mirror assembly;

sense circuitry coupled to the sense capacitor, including a sense pulse generator providing a first polarity sense pulse and a second

polarity sense pulse, said sense pulse generator coupled to said sense capacitor;

a storage device coupled to the sense circuitry; and

a demodulator coupled to said storage device.

42. The optical mirror switch of claim 41 further including a plurality of sense capacitors coupled to the optical mirror, at least a first set of said plurality coupled to detect a position change in said mirror in a first direction and a second set of said plurality coupled to detect a position change in a second direction.

43. The optical mirror switch of claim 41 wherein said sense circuitry includes a charge detector.

44. The optical mirror switch of claim 41 wherein said sense circuitry includes a charge integrator.

45. A method of operating a switched-capacitor circuit, comprising:

providing a plurality of sense pulses having a first polarity to a sense capacitor during a first phase to obtain a first output of the sense transducer; and

providing a plurality of sense pulses having a second polarity to a sense capacitor during a second phase to obtain a second output of the sense transducer.

46. The method of claim 45 further including the step of storing the output of the sense capacitor.

47. The method of claim 45 further including the step of sampling an output of the sense capacitor

48. The method of claim 47 further including demodulating the output of the first and the second phases.

49. An improved capacitive sensing circuit comprising:

a sense pulse generator providing a first magnitude sense pulse and a second magnitude sense pulse;

a sense capacitor coupled to the sense pulse generator;

a charge detector coupled to the sense capacitor;

a storage device coupled to the charge detector; and

a demodulator coupled to the storage device.